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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,518	12/12/2003	Michel Marty	S1022.881073US00	1577

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EXAMINER	
WILSON, CHRISTIAN D	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 08/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,518	MARTY ET AL.	
	Examiner	Art Unit	
	Christian Wilson	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *8 and 9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 8 and 9 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on December 22, 2004.

Specification

2. The objections to the specification are withdrawn.

Claim Rejections - 35 USC § 112

3. The rejections of claims 1 – 7 under 35 U.S.C. 112 are withdrawn.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 15 recites the limitation "gluing". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1 – 7 and 10 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaul *et al.* in view of Delgado *et al.*

Gaul *et al.* (US 5,807,783) teaches a method of manufacturing buried connections comprising the steps of providing a structure formed of a first support wafer **12** glued onto a rear surface **6** of a thin semiconductor wafer **10** with a semiconductor element **20** formed in and above the semiconductor wafer, gluing a second support layer wafer **40** on the front surface of the thin semiconductor wafer, removing the first support wafer [Figure 7], forming interconnections **38** between opened areas of the rear surface of the semiconductor wafer, and removing the second support wafer [column 6, line 32]. Gaul *et al.* does not explicitly discuss gluing a third support wafer to the interconnections, but does describe the compatibility of Delgado *et al.* (US 5,091,331) with the current process [column 6, lines 40-50]. Delgado *et al.* teaches gluing a third support wafer on the interconnections [Figure 7]. It would have been obvious to one of ordinary skill in the art to use the third support wafer of Delgado *et al.* in the method of Gaul *et al.* since this wafer provides improved support during the dicing process [column 1, lines 35-45].

Regarding claim 2, Gaul *et al.* further teaches gluing using an insulating layer **14**.

Regarding claim 3, Gaul *et al.* further teaches etching open areas in the insulating layer and filling the open areas with a conductive material [Figure 8].

Regarding claim 4, Gaul *et al.* further teaches producing areas of reduced thickness in the insulating layer [column 5, lines 40-45].

Regarding claim 5, Gaul *et al.* further teaches depositing a metal layer and forming a silicide layer [column 5 , lines 45-55], but does not discuss an annealing process. It would have been obvious to one of ordinary skill in the art to use an annealing process to form the silicide layer since this is a well known method in semiconductor manufacturing.

Regarding claim 6, Gaul *et al.* further teaches covering the surface of the conductive material with a second insulating layer [column 7, lines 1-5]. Gaul *et al.* does not discuss using CMP to expose the insulating layer, but does discuss CMP to thin device layers [column 4, lines 20-25]. It would have been obvious to one of ordinary skill in the art to use CMP to planarize the conductive filling material since this is a well known planarization process for metals.

Regarding claim 7, Gaul *et al.* further teaches covering the structure with a bonding layer **31**.

Regarding claim 10, Gaul *et al.* teaches a method of manufacturing buried connections comprising the steps of attaching a first support wafer **12** glued onto a first surface **6** of a thin semiconductor wafer **10**, attaching a second support layer wafer **40** on the second surface of the thin semiconductor wafer, removing the first support wafer [Figure 7], forming interconnections **38** between opened areas of the rear surface of the semiconductor wafer, and removing the second support wafer [column 6, line 32]. Gaul *et al.* does not explicitly discuss attaching a third support wafer to the interconnections, but does describe the compatibility of Delgado *et al.* (US

5,091,331) with the current process [column 6, lines 40-50]. Delgado *et al.* teaches attaching a third support wafer on the interconnections [Figure 7]. It would have been obvious to one of ordinary skill in the art to use the third support wafer of Delgado *et al.* in the method of Gaul *et al.* since this wafer provides improved support during the dicing process [column 1, lines 35-45].

Regarding claim 11, Gaul *et al.* further teaches attaching using an insulating layer **14**.

Regarding claim 12, Gaul *et al.* further teaches etching open areas in the insulating layer and filling the open areas with a conductive material [Figure 8].

Regarding claim 13, Gaul *et al.* further teaches producing areas of reduced thickness in the insulating layer [column 5, lines 40-45].

Regarding claim 14, Gaul *et al.* further teaches depositing a metal layer and forming a silicide layer [column 5 , lines 45-55], but does not discuss an annealing process. It would have been obvious to one of ordinary skill in the art to use an annealing process to form the silicide layer since this is a well known method in semiconductor manufacturing.

Regarding claim 15, Gaul *et al.* further teaches covering the surface of the conductive material with a second insulating layer [column 7, lines 1-5]. Gaul *et al.* does not discuss using CMP to expose the insulating layer, but does discuss CMP to thin device layers [column 4, lines 20-25]. It would have been obvious to one of ordinary skill in the art to use CMP to planarize the conductive filling material since this is a well known planarization process for metals.

Regarding claim 16, Gaul *et al.* further teaches covering the structure with a bonding layer **31**.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian Wilson whose telephone number is (571) 272-1886. The examiner can normally be reached on weekdays, 7:30 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christian Wilson, Ph.D.
Primary Examiner
Art Unit 2891

CDW